IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method of operating a memory device, comprising:

receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein receiving the F-bit word comprises:

receiving a ~~first subset of a set of command and address signals~~ first portion of the F-bit word substantially simultaneous with receiving a first edge of a clock signal, wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein the G-bit portion comprises a first subset of a set of command and address signals; and

receiving a ~~second subset of the set of command and address signals~~ second portion of the F-bit word substantially simultaneous with receiving a second edge of the clock signal, wherein the second portion of the F-bit word comprises H-bits, wherein H is F-G, wherein the H-bit portion comprises a second subset of the set of command and address signals; and

performing a memory command in response to the ~~set of command and address signals~~ received F-bit word.

2. (Currently Amended) The method of claim 1, wherein the memory device comprises a device selected from the group consisting of a DRAM device, a flash memory device, ~~a volatile memory device,~~ a non-volatile memory device, a static random access memory (SRAM) device, and a static memory device.

3. (Currently Amended) The method of claim 1, further comprising:

sending the first ~~subset of the set of command and address signals~~ portion of the F-bit word substantially simultaneous with sending the first edge of the clock signal by an external controller; and

sending the second ~~subset of the set of command and address signals~~ portion of the F-bit word substantially simultaneous with sending the second edge of the clock signal by the external controller.

4. (Original) The method of claim 3, wherein, in sending, the external controller is a device selected from the group consisting of a DRAM controller, a central processing unit (CPU), a graphics processing unit (GPU), and a processor.

5. (Currently Amended) A method of operating a memory device, comprising:

receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein receiving the F-bit word comprises:

receiving a ~~set of command signals and a first subset of a set of address signals~~ first portion of the F-bit word substantially simultaneous with receiving a first edge of a clock signal, wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein the G-bit portion comprises a set of command signals and a first subset of a set of address signals; and

receiving a ~~second subset of the set of address signals~~ second portion of the F-bit word substantially simultaneous with receiving a second edge of the clock signal, wherein the second portion of the F-bit word comprises H-bits, wherein H is F-G, wherein the H-bit portion comprises a second subset of the set of address signals; and

performing a memory command in response to the ~~set of command and address signals~~ received F-bit word.

6. (Currently Amended) The method of claim 5, wherein the memory device comprises a device selected from the group consisting of a DRAM device, a flash memory device, ~~a volatile memory device,~~ a non-volatile memory device, a static random access memory (SRAM) device, and a static memory device.

7. (Original) The method of claim 5, wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, wherein in the rising and falling edges

comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively.

8. (Currently Amended) A method of operating a memory device, comprising:

receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein receiving the F-bit word comprises:

receiving a ~~first subset of a set of command and address signals~~ first portion of the F-bit word substantially simultaneous with receiving a first edge of a first cycle of a clock signal, wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein the G-bit portion comprises a first subset of a set of command and address signals; and

receiving a ~~second subset of the set of command and address signals~~ second portion of the F-bit word substantially simultaneous with receiving a first edge of a second cycle of the clock signal, wherein the second portion of the F-bit word comprises H-bits, wherein H is F-G, wherein the H-bit portion comprises a second subset of the set of command and address signals; and

performing a memory command in response to the ~~set of command and address signals~~ received F-bit word.

9. (Currently Amended) The method of claim 8, wherein, in receiving the ~~second subset of command and address signals~~ second portion of the F-bit word, the second cycle is substantially subsequent to the first cycle.

10. (Currently Amended) The method of claim 8, wherein the memory device ~~comprising~~ comprises a device selected from the group consisting of a DRAM device, a flash memory device, ~~a volatile memory device,~~ a non-volatile memory device, a static random access memory (SRAM) device, and a static memory device.

11. (Currently Amended) A method of operating a memory device, comprising:

receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein receiving the F-bit word comprises:

receiving a ~~set of command signals and a first subset of a set of address signals~~ first portion of the F-bit word substantially simultaneous with receiving a first edge of a first cycle of a clock signal, wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein the G-bit portion comprises a set of command signals and a first subset of a set of address signals; and

receiving a ~~second subset of the set of address signals~~ second portion of the F-bit word substantially simultaneous with receiving a first edge of a second clock cycle of the clock signal, wherein the second portion of the F-bit word comprises H-bits, wherein H is F-G, wherein the H-bit portion comprises a second subset of the set of address signals; and

performing a memory command in response to the ~~set of command and address signals~~ received F-bit word.

12. (Currently Amended) The method of claim 11, wherein, in receiving the ~~second subset of the set of address signals~~ second portion of the F-bit word, the second cycle is substantially subsequent to the first cycle.

13. (Currently Amended) The method of claim 11, wherein a clock signal comprises a first and second edge, wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively.

14. (Currently Amended) The method of claim 11, wherein the memory device ~~comprising~~ comprises a device selected from the group consisting of a DRAM device, a flash memory device, ~~a volatile memory device,~~ a non-volatile memory device,-a static random access operating memory (SRAM) device, and a static memory device.

15. (Currently Amended) A memory device comprising:

multiple command and address pins to receive a ~~first subset of a set of command and address signals~~ first portion of an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the first portion of the F-bit word comprises a first subset of the set of command and address signals, wherein the multiple command and address pins receive the first portion of the F-bit word substantially simultaneous with receiving a first edge of a clock signal, wherein the multiple command and address pins to further receive a ~~second subset of the set of command and address signals~~ second portion of an F-bit word, wherein the second portion of the F-bit word comprises a second subset of the set of command and address signals, wherein the multiple command and address pins receive the second portion of the F-bit word substantially simultaneous with receiving a second edge of a clock signal, and wherein the memory device operates to perform a memory command in response to the ~~set of received command and address signals~~ received F-bit word.

16. (Currently Amended) The memory device of claim 15, wherein the memory device is a device selected from the group consisting of a DRAM device, a flash memory device, ~~a volatile memory device,~~ a non-volatile memory device, a static random access memory (SRAM) device, and a static memory device.

17. (Original) The memory device of claim 15, wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, respectively, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively.

18. (Currently Amended) A memory device comprising:

multiple command and address pins to receive a ~~first subset of a set of command and address signals~~ first portion of an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the first portion of the F-bit word comprises a first subset of the set of command and address signals, wherein the multiple command and address pins receive the first portion of the F-bit word substantially simultaneous

with receiving a first edge of a first cycle of a clock signal, wherein the multiple command and address pins to further receive a ~~second subset of the set of command and address signals~~ second portion of an F-bit word, wherein the second portion of the F-bit word comprises a second subset of the set of command and address signals, wherein the multiple command and address pins receive the second portion of the F-bit word substantially simultaneous with receiving a first edge of a second cycle of the clock signal, and wherein the memory device to perform a memory command in response to the ~~set of received command and address signals~~ received F-bit word.

19. (Currently Amended) The memory device of claim 18, wherein the memory device is a device selected from the group consisting of a DRAM device, a flash memory device, ~~a volatile memory device,~~ a non-volatile memory device, a static random access memory (SRAM) device, and a static memory device.

20. (Currently Amended) The memory device of claim 18, wherein a clock signal comprises a first and second edge, wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, respectively, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively.

21. (Currently Amended) A memory circuit comprising:

one or more integrated circuit memory devices operable for communicating with an external controller, wherein each of the integrated circuit memory devices operates to receive a ~~first subset of a set of command and address signals~~ first portion of an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the first portion of the F-bit word comprises a first subset of the set of command and address signals, wherein the multiple command and address pins receive the first portion of the F-bit word substantially simultaneous with receiving a first edge of a clock signal, wherein each of the integrated memory circuit devices operates to receive a ~~second subset of the set of command and address signals~~ second portion of an F-bit word, wherein the second portion of the F-bit word comprises a second subset of the set of command and address signals, wherein the

multiple command and address pins receive the second portion of the F-bit word substantially simultaneous with receiving a second edge of a clock signal, and wherein each integrated circuit memory device operates to perform a memory command in response to the ~~set of received associated command and address signals~~ received F-bit word.

22. (Original) The memory circuit of claim 21, wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, respectively, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively.

23. (Currently Amended) The memory circuit of claim 21, wherein the integrated circuit memory device is a memory device selected from the group consisting of a DRAM device, a flash memory device, ~~a volatile memory device,~~ a non-volatile memory device, a SRAM device, and a static memory device.

24. (Currently Amended) A memory circuit comprising:

one or more integrated circuit memory devices operable for sending and receiving signals, wherein each of the integrated circuit memory devices operates to receive a ~~first subset of a set of command and address signals~~ first portion of an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the first portion of the F-bit word comprises a first subset of the set of command and address signals, wherein the multiple command and address pins receive the first portion of the F-bit word substantially simultaneous with receiving a first edge of a first cycle of a clock signal, wherein each of the integrated memory circuit devices operates to further receive a ~~second subset of the set of command and address signals~~ second portion of an F-bit word, wherein the second portion of the F-bit word comprises a second subset of the set of command and address signals, wherein the multiple command and address pins receive the second portion of the F-bit word substantially simultaneous with receiving a first edge of a second cycle of the clock signal, and wherein each integrated circuit memory device operates to perform a memory command in response to the ~~set of received associated command and address signals~~ received F-bit word.

25. (Currently Amended) The memory circuit of claim ~~24wherein~~ 24, wherein the second cycle is substantially subsequent to the first cycle in the clock signal.

26 (Currently Amended) The memory circuit of claim 24, wherein a clock signal comprises a first and second edge, wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, respectively, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively.

27. (Currently Amended) The memory circuit of claim 24, wherein the integrated circuit memory device is a memory device selected from the group consisting of a DRAM device, a flash memory device, ~~a volatile memory device,~~ a non-volatile memory device, a SRAM device, and a static memory device.

28. (Currently Amended) A system comprising:

one or more integrated circuit memory devices, wherein each of the one or more integrated circuit memory devices includes multiple data, command, and address pins; and

a bus, wherein the one or more integrated circuit memory devices are coupled via the bus to a controller through the multiple data, command, and address pins, wherein the controller operates to send a word comprising command and address signals during a clock cycle of a clock signal such that the number of ~~command and address signals~~ bits in the word sent from the controller to the integrated circuit memory device is higher than a given number of command and address pins in each integrated circuit memory device.

29. (Original) The system of claim 28, wherein the controller is selected from the group consisting of a DRAM controller, a central processing unit (CPU), a graphics processing unit (GPU), and a processor.

30. (Currently Amended) The system of claim 28, wherein the integrated circuit memory device is a memory device selected from the group consisting of a DRAM device, a flash

memory device, ~~a volatile memory device,~~ a non-volatile memory device,~~-~~a SRAM device, and a static memory device.

31. (Original) The system of claim 28, wherein the controller is operable for sending the command and address signals during the clock cycle of the clock signal comprises sending the command and address signals upon both rising and falling edges of the clock cycle when transferring data to and from each integrated circuit memory device.

32. (Currently Amended) A semiconductor circuit comprising:

one or more integrated circuit memory devices, wherein each integrated circuit memory device comprises multiple command and address pins, wherein the command and address pins of each integrated circuit memory device are coupled to receive words comprising command and address signals, wherein the memory devices ~~operates~~ operate to receive ~~command and address signals~~ words during a clock cycle of a clock signal such that the number of ~~command and address signals~~ bits in the words sent to each integrated circuit memory device is higher than the multiple command and address pins available in each integrated circuit memory device.

33. (Currently Amended) The semiconductor circuit of claim 32, wherein the integrated circuit memory device is a memory device selected from the group consisting of a DRAM device, a flash memory device, ~~a volatile memory device,~~ a non-volatile memory device, a SRAM device, and a static memory device.

34. (Currently Amended) The semiconductor circuit of claim 32, wherein the command and address signals during the clock cycle of the clock signal ~~is~~ are ~~selected~~ initiated from the group consisting of initiating the command and address signals upon both the rising and falling edges of the clock cycle of the clock signal, initiating the command and address signals upon a rising edge of the clock cycle and further initiating address signals on a falling edge of the ~~timing~~ clock cycle, initiating the command and address signals upon two consecutive rising edges of the ~~timing~~ clock signal, and initiating the command and address signals on a rising edge of the

~~timing~~ clock cycle and further initiating the address signals on a subsequent rising edge of the ~~timing~~ clock cycle.

35. (Canceled)

36. (Currently Amended) A memory circuit comprising:

one or more integrated circuit memory devices, wherein each integrated circuit memory device comprises a predetermined number of command and address pins, wherein each integrated circuit memory device is coupled to send and receive signals on the predetermined number of command and address pins, wherein the one or more memory devices operates to receive a word comprising a number of command and address signals during more than one edge of a clock signal such that the number of ~~command and address signals~~ bits in each word for each integrated circuit memory device are substantially higher than the predetermined number of command and address pins in each integrated circuit memory device.

37. (Original) The memory circuit of claim 36, wherein the integrated circuit memory device is a DRAM device.

38. (Currently Amended) The memory circuit of claim 36, wherein the command and address signals are ~~selected~~ initiated from the group consisting of initiating the command and address signals upon both the rising and falling edges of the clock cycle of the clock signal, initiating the command and address signals upon a rising edge of the clock cycle and further initiating address signals on a falling edge of the ~~timing~~ clock cycle, initiating the command and address signals upon two consecutive rising edges of the ~~timing~~ clock signal, and initiating the command and address signals on a rising edge of the ~~timing~~ clock cycle and further initiating the address signals on a subsequent rising edge of the ~~timing~~ clock cycle.

39. (New) The method of claim 1, wherein the integrated circuit memory device is a volatile memory device.

40. (New) The method of claim 5, wherein the integrated circuit memory device is a volatile memory device.

41. (New) The method of claim 8, wherein the integrated circuit memory device is a volatile memory device.

42. (New) The method of claim 11, wherein the integrated circuit memory device is a volatile memory device.

43. (New) The memory device of claim 15, wherein the integrated circuit memory device is a volatile memory device.

44. (New) The memory device of claim 18, wherein the integrated circuit memory device is a volatile memory device.

45. (New) The memory circuit of claim 21, wherein the integrated circuit memory device is a volatile memory device.

46. (New) The memory circuit of claim 24, wherein the integrated circuit memory device is a volatile memory device.

47. (New) The system of claim 28, wherein the integrated circuit memory device is a volatile memory device.

48. (New) The semiconductor circuit of claim 32, wherein the integrated circuit memory device is a volatile memory device.

49. (New) A method, comprising:

receiving an F-bit word using J command and address pins of a programmable memory device, wherein F and J are positive integers, wherein J is less than F, wherein the F-bit word comprises a set of command and address signals, comprising:

receiving a first portion of the F-bit word at a first time, wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein G is less than or equal to J;

receiving a second portion of the F-bit word at a second time, wherein the second portion of the F-bit word comprises H-bits, wherein H is F-G, wherein H is less than or equal to J; and

performing a memory command in response to the fully-received F-bit word.

50. (New) The method of claim 49, wherein a first time includes at or substantially simultaneously with receiving a first edge of a clock signal.

51. (New) The method of claim 50, wherein the first edge of a clock signal includes a first edge of a first cycle of the clock signal.

52. (New) The method of claim 51, wherein the first edge is a rising edge of the clock signal.

53. (New) The method of claim 52, wherein the first edge is a falling edge of the clock signal.

54. (New) The method of claim 49, wherein a second time includes at or substantially simultaneously with receiving a second edge of a clock signal.

55. (New) The method of claim 54, wherein the second edge of a clock signal includes a first edge of a second cycle of the clock signal.

56. (New) The method of claim 55, wherein the second edge is a rising edge of the clock signal.

57. (New) The method of claim 56, wherein the second edge is a falling edge of the clock signal.

58. (New) The method of claim 49, wherein the G-bit portion of the F-bit word comprises command and address signals.

59. (New) The method of claim 58, wherein the command and address signals comprise a first subset of a set of command and address signals.

60. (New) The method of claim 58, wherein the command and address signals comprise a set of command signals and a first subset of a set of address signals.

61. (New) The method of claim 49, wherein the H-bit portion of the F-bit word comprises address signals.

62. (New) The method of claim 61, wherein the address signals comprise a second subset of a set of address signals.

63. (New) The method of claim 49, wherein the H-bit portion of the F-bit word comprises command and address signals.

64. (New) The method of claim 63, wherein the command and address signals comprise a second subset of a set of command and address signals.

65. (New) The method of claim 49, wherein a programmable memory device includes a device selected from the group consisting of a dynamic random access memory (DRAM) device,

a static random access memory (SRAM) device, a static memory device, a flash memory device, and a non-volatile memory device.

66. (New) The method of claim 49, wherein a programmable memory device includes a volatile memory device.

67. (New) The method of claim 49, further comprising:
sending the first portion of the F-bit word with a controller at a first time; and
sending the second portion of the F-bit word with a controller at a second time.

68. (New) The method of claim 67, wherein a controller is a device selected from the group consisting of a DRAM controller, a central processing unit (CPU), a graphics processing unit (GPU), and a processor.

69. (New) The method of claim 67, wherein a first time includes at or substantially simultaneously with receiving a first edge of a clock signal.

70. (New) The method of claim 69, wherein the first edge of a clock signal includes a first edge of a first cycle of the clock signal.

71. (New) The method of claim 70, wherein the first edge is a rising edge of the clock signal.

72. (New) The method of claim 71, wherein the first edge is a falling edge of the clock signal.

73. (New) The method of claim 67, wherein a second time includes at or substantially simultaneously with receiving a second edge of a clock signal.

74. (New) The method of claim 73, wherein the second edge of a clock signal includes a first edge of a second cycle of the clock signal.

75. (New) The method of claim 74, wherein the second edge is a rising edge of the clock signal.

76. (New) The method of claim 75, wherein the second edge is a falling edge of the clock signal.

77. (New) The method of claim 49, wherein H and G are not equal to each other.

78. (New) The method of claim 49, wherein a programmable memory device consists of J command and address pins.

79. (New) The method of claim 49, wherein address signals consist of row address data.